

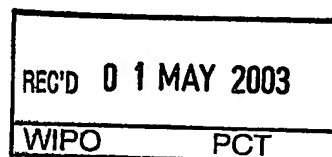
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Date of Filing : 30 SEPTEMBER 2002 (30-09-2002)  
Application number : 200205929-3  
Applicants : INFINEON TECHNOLOGIES AG  
Title of Invention : SWITCHING MODE POWER SUPPLIES

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23 April 2003

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**PATENTS FORM 1**  
Patents Act  
(Cap. 221)  
Patents Rules  
Rule 19

**INTELLECTUAL PROPERTY OFFICE OF SINGAPORE**  
**REQUEST FOR THE GRANT OF A PATENT UNDER**  
**SECTION 25**



101101

\* denotes mandatory fields

**1. YOUR REFERENCE\***

SP5288

**2. TITLE OF INVENTION\***

SWITCHING MODE POWER SUPPLIES

**3. DETAILS OF APPLICANT(S)\* (see note 3)**

Number of applicant(s)

1

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For corporate applicant



For individual applicant

State of Incorporation

State of residency

Country of Incorporation

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Country of residency



For others (please specify in the box provided below)

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30 SEP 2002

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State of residency

Country of incorporation

Country of residency

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State

Country

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☐ For others (please specify in the box provided below)

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Further applicants are to be indicated on continuation sheet 1

#### 4. DECLARATION OF PRIORITY (see note 5)

A. Country/country designated

DD MM YYYY

File number

Filing Date

B. Country/country designated

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File number

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Further details are to be indicated on continuation sheet 6

#### 5. INVENTOR(S)\* (see note 6)

A. The applicant(s) is/are the sole/joint inventor(s)

Yes

☐

No

☒

200205929-3  
30 SEP 2002

B. A statement on Patents Form 8 is/will be furnished

Yes

☒

No

☐

**6. CLAIMING AN EARLIER FILING DATE UNDER (see note 7)**

☐

section 20(3)

☐

section 26(6)

☐

section 47(4)

Patent application number

DD MM YYYY

Filing Date

Please mark with a cross in the relevant checkbox provided below  
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Proceedings under rule 27(1)(a)

DD MM YYYY

Date on which the earlier application was amended

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Proceedings under rule 27(1)(b)

**7. SECTION 14(4)(C) REQUIREMENTS (see note 8)**

Invention has been displayed at an international exhibition. Yes

☐

No

☒

**8. SECTION 114 REQUIREMENTS (see note 9)**

The invention relates to and/or used a micro-organism deposited for the purposes of disclosure in accordance with section 114 with a depository authority under the Budapest Treaty.

Yes

☐

No

☒

**9. CHECKLIST\***

(A) The application consists of the following number of sheets

i.	Request	<input type="text" value="5"/>	Sheets
ii.	Description	<input type="text" value="12"/>	Sheets
iii.	Claim(s)	<input type="text" value="3"/>	Sheets
iv.	Drawing(s)	<input type="text" value="8"/>	Sheets
v.	Abstract (Note: The figure of the drawing, if any, should accompany the abstract)	<input type="text" value="1"/>	Sheets
Total number of sheets		<input type="text" value="29"/>	Sheets

(B) The application as filed is accompanied by:

☐

Priority document(s)

☐

Translation of priority document(s)

☐

Statement of inventorship  
& right to grant

☐

International exhibition certificate

10. DETAILS OF AGENT (see notes 10, 11 and 12)

Name

Firm

LLOYD WISE

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12. NAME, SIGNATURE AND DECLARATION (WHERE APPROPRIATE) OF APPLICANT OR AGENT\* (see note 12)  
(Note: Please cross the box below where appropriate.)

☒

I, the undersigned, do hereby declare that I have been duly authorised to act as representative, for the purposes of this application, on behalf of the applicant(s) named in paragraph 3 herein.

Lloyd Wise  
Name and Signature LLOYD WISE

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27 09 2002

Our Ref: SP5288

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1. This form when completed, should be brought or sent to the Registry of Patents together with the rest of the application. Please note that the filing fee should be furnished within the period prescribed.
2. The relevant checkboxes as indicated in bold should be marked with a cross where applicable.
3. Enter the name and address of each applicant in the spaces provided in paragraph 3.  
Where the applicant is an individual
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Where the applicant is a body corporate
  - Bodies corporate should be designated by their corporate name and country of incorporation and, where appropriate, the state of incorporation within that country should be entered where provided.
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Where the applicant is a partnership
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4. In the field for "Country", please refer to the standard list of country codes made available by the Registry of Patents and enter the country code corresponding to the country in question.
5. The declaration of priority in paragraph 4 should state the date of the previous filing, the country in which it was made, and indicate the file number, if available. Where the application relied upon in an International Application or a regional patent application e.g. European patent application, one of the countries designated in that application [being one falling under section 17 of the Patents Act] should be identified and the country should be entered in the space provided.
6. Where the applicant or applicants is/are the sole inventor or the joint inventors, paragraph 5 should be completed by marking with a cross the 'YES' checkbox in the declaration (A) and the 'NO' checkbox in the alternative statement (B). Where this is not the case, the 'NO' checkbox in declaration (A) should be marked with a cross and a statement will be required to be filed on Patents Form 8.
7. When an application is made by virtue of section 20(3), 26(6) or 47(4), the appropriate section should be identified in paragraph 6 and the number of the earlier application or any patent granted thereon identified. Applicants proceeding under section 26(6) should identify which provision in rule 27 they are proceeding under. If the applicants are proceeding under rule 27(1)(a), they should also indicate the date on which the earlier application was amended.
8. Where the applicant wishes an earlier disclosure of the invention by him at an International Exhibition to be disregarded in accordance with section 14(4)(c), then the 'YES' checkbox at paragraph 7 should be marked with a cross. Otherwise, the 'NO' checkbox should be marked with a cross.
9. Where in disclosing the invention the application refers to one or more micro-organisms deposited with a depository authority under the Budapest Treaty, then the 'YES' checkbox at paragraph 8 should be marked with a cross. Otherwise, the 'NO' checkbox should be marked with a cross. Attention is also drawn to the Fourth Schedule of the Patents Rules.
10. Where an agent is appointed, the fields for "DETAILS OF AGENT" and "ADDRESS FOR SERVICE IN SINGAPORE" should be completed and they should be the same as those found in the corresponding Patents Form 41. In the event where no agent is appointed, the field for "ADDRESS FOR SERVICE IN SINGAPORE" should be completed, leaving the field for "DETAILS OF AGENT" blank.
11. In the event where an individual is appointed as an agent, the sub-field "Name" under "DETAILS OF AGENT" must be completed by entering the full name of the individual. The sub-field "Firm" may be left blank. In the event where a partnership/body corporate is appointed as an agent, the sub-field "Firm" under "DETAILS OF AGENT" must be completed by entering the name of the partnership/body corporate. The sub-field "Name" may be left blank.
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30 SEP 2002  
200205929-3

Switching mode power suppliesField of the invention

The present invention relates to switching mode power supplies (SMPS), and in particular to a control circuit for a SMPS, to a SMPS itself, to apparatus  
5 powered by and incorporating the SMPS and to methods performed by the SMPS and the control circuit.

Background of the invention

Switching mode power supplies are being increasingly used in many domestic and industrial applications. Apparatus such as televisions or computer monitors  
10 operate in one of a number of states or modes. For example, a first "off" mode occurs when there is no power being supplied to the apparatus; a second "on" mode occurs when the device is switched on and operating normally; and a third mode, referred to as a "standby mode", occurs when the device is to remain powered but with reduced functions and reduced power consumption. In  
15 the case that the apparatus is a television, for example, the standby mode may, for example, be a mode in which the television is not displaying a picture or producing sound, but certain circuitry in the television remains powered so that, if the "on" button of the remote control is pressed the television will return to the "on" mode.

20 SMPS are implemented by supplying a regulated power supply to a the primary side of a transformer in series with a transistor. The secondary side of the transformer is connected to the apparatus ("load"). Switching of the transistor (usually, but not exclusively, switching off of the transistor; so called "fly-back" operation) causes variations in the current through the transformer, resulting in  
25 an output power on the secondary side of the transistor. The secondary side of the transformer is connected via a smoothing circuit to the apparatus to be powered. The average number of switching operations per unit time, and the current caused to flow in the transistor in each switching operation, together  
30 determine the average power transmitted to the apparatus. The main

advantage of SMPS in comparison to conventional power supplies built up by means of linear regulators is their high efficiency at full load.

However, when the load decreases and the switching cycle remains the same, the efficiency of the SMPS decreases tremendously, since power losses are almost entirely due to the switching losses, which in turn are almost exactly proportional to the number of switching operations the transistor performs. A known solution to this problem is to reduce the number of switching operations per unit time as the load falls, such that the average number of switching operations is sufficient to supply the load. Since the number of switching operations is reduced, the switching losses decrease as the load is reduced.

There are several known methods for controlling the timing of the switching operations.

One solution is "frequency reduction", in which in a given mode the switching operations on the transistor are periodic with a frequency substantially proportional to the power to be supplied to the load in that mode. Thus, in modes for which the power consumption of the load is low, the frequency of the switching operation is low, and thus the switching losses are low. Such a solution is described for example in the document "Data sheet TEA1507", published by Philips on 5 December 2000. A disadvantage of this technique is that if the frequency of the switching operations decreases into the audible range, an audible noise is generated by the transformer.

Another solution is to maintain the frequency of the switching operations at the same value irrespective of whether the device is operating in high or low power mode, but in the low power mode to interrupt the switching operations. Thus, in this "burst mode" there are "bursts" ("frames") of high frequency power pulses separated by periods in which there are no power pulses at all. The average power transmitted thus depends upon the proportion of the operation of the SMPS for which the bursts are transmitted. Such techniques too are described in the TEA1507 document. US639206 also describes such a concept. The burst

mode is entered by a signal generated from the secondary side of the transformer, and transmitted to the primary side by an optocoupler. Once, the burst mode is entered, the timing of the bursts is determined by a measurement of a voltage ("undervoltage") on the primary side. This is known as  
5 "undervoltage lockout". A disadvantage of this technique is that if the load rises during one of the periods between bursts then the circuit cannot react until the next burst is reached.

Another known technique is to control the burst mode based on a Vcc signal  
10 derived from a winding on the transformer. This is employed in the FS6Series of Fairchild (see, for example, application note 4116 published by Fairchild Semiconductor Corporation). The burst mode is entered if a feedback signal obtained from the secondary side of the transformer is kept below a certain level. The disadvantage with this is that the control is mainly taken over by the  
15 Vcc and therefore not directly load dependent.

Another known technique, employed in US6385061B1 and in the NCP1203 system of Semiconductor Component Industries LLC, is to start the burst mode when the load is below a certain level. The disadvantage of this concept is that  
20 there is no hysteresis implemented between the normal operation mode and the burst mode. Therefore, high frequency turning on and off of the burst mode (high frequency "bursting") can occur if the changes around this level become small, and this too can lead to a disadvantageous audible noise.

## 25 Summary of the invention

A first aspect of the present invention proposes in general terms that an input received from the secondary side of the transformer and indicative of the power being drawn by the load is used to control the timing of bursts. The input is  
30 compared with two different threshold values, and the burst mode is switched on if the input rises above a first higher threshold value, and switched off if it falls below a second lower threshold value.

The invention thus makes it possible to determine the duty cycle and the frequency of a burst mode only from a feedback signal which contains the load information from the SMPS. The difference between the two threshold values gives a hysteresis, which removes high frequency bursting.

5

Specifically, one expression of the first aspect of the invention is a switching mode power supply having a transformer, a transistor controlling the current through the primary of the transformer, and a control unit for controlling the switching of the transformer to generate current pulses in the transformer, the control unit being arranged to receive a signal from the secondary side of the transformer and compare it with two threshold levels defining a range, the control unit enabling switching of the transistor in the case that the signal is outside the range in a first direction, and disabling switching of the transistor in the case that the signal is outside the range in a second direction.

10 In a second aspect, the present invention proposes in general terms that a measurement is made indicative of the current through the gate, and that in the burst mode the switching of the transistor is controlled to limit this current.

The second aspect of the invention is motivated by an observation that, irrespective of the bursting frequency, noise may be generated in the transformer if the current which flows through it is too great.

Specifically, one expression of the second aspect of the invention is a switching mode power supply having a transformer, a transistor controlling the current through the primary of the transformer, a control unit for controlling the switching of the transformer to generate current pulses in the transformer, a memory device for storing data indicating whether the switching mode power supply is operating in a certain power supply mode, and a current limitation circuit arranged to receive a signal indicative of the current through the primary of the transformer and to limit the current pulse if the signal indicates that the current is above a threshold value and the memory device indicates that the switching mode power supply is operating in said power supply mode.

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### Brief description of the figures

Further preferred features of the invention will now be described for the sake of  
5 example only with reference to the following figures, in which:

Fig. 1 shows a circuit diagram of a first embodiment of the invention;

Fig. 2 (a) shows a preferred implementation of the second embodiment of the invention in which the signal is directly related to the power drawn by the load;

Fig. 2 (b) shows an alternate implementation of the second embodiment of the invention of Fig. 2 (a) in which the signal is inversely related to the power drawn  
10 by the load;

Fig. 3 shows waveforms observed in the embodiment of Fig. 2 (a);

Fig. 4 shows the profiles of current spikes in the embodiment of Fig. 2 (a);

Fig. 5, which is composed of Figs. 5(a)-5(c), illustrates the variation of burst  
15 frequency with load in the embodiment of Fig. 2 (a);

Fig. 6 shows a third embodiment of the invention;

Fig. 7 shows a fourth embodiment of the invention; and

Fig. 8 shows waveforms observed in the embodiment of Fig. 7.

### Detailed description of the embodiments

20 Fig. 1 shows schematically a power converter which is a first embodiment of the invention. An AC voltage supply  $V_{in}$  is received at the left of the figure. Typically  $V_{in}$  is in the range 85 to 270V. It is rectified by a rectifier 3, and then passed to a smoothing capacitor 5. The DC voltage thus generated is fed to one input of a transformer 7 having a primary winding 9 and a secondary winding 11. A  
25 snubber 13 is connected between the two inputs of the primary winding 9, and the other common connection of the snubber 13 and primary winding 9 is

connected to an input of a transistor 15. The gate of the transistor 15 is controlled by an output called "Gate" of a control system 1. The other side of the transistor 15 is connected to ground via a resistor  $R_{\text{sense}}$ . The voltage at one side of the resistor  $R_{\text{sense}}$  is an input CS to the control system 1. The control system 1 further receives an input HV from the rectifier 3 for powering the unit 1. When in standby mode, the input HV serves as a current source that can be switched off for current conservation. The control system 1 also receives an input  $V_{\text{CC}}$  from one side of an additional winding 17, other side of winding 17 being connected to ground. The input  $V_{\text{CC}}$  is smoothed by a capacitor  $C_{\text{VCC}}$ .

The secondary winding 11 of the transformer 7 is connected via a diode 19 across a p-filter, formed by smoothing capacitors 21 and 25 and an inductor 23, to give a DC voltage output  $V_{\text{out}}$ . The secondary side of the transformer 7 is further provided with circuitry 27 of a conventional design (described for example in the reference US6385061), including an optocoupler 29, in which current through a light emitting diode 31 is detected by a light sensitive element 33, which is connected between ground and a signal input FB of the control system 1.

The control system 1 further includes a connection GND to ground, and a connection SoftS to ground via a capacitor  $C_{\text{SoftS}}$ .

The control system 1 includes the following units: a start-up cell 35 connected to HV and providing current to  $V_{\text{CC}}$ . A power management unit 37, controlling the startup cell 35 and receiving the signal  $V_{\text{CC}}$ . A pulse width modulator (PWM) 39, receiving the input CS and generating the output Gate, and a control unit 41. The control unit 41 receives an input from the power management unit 37 and the PWM unit 39, and transmits outputs to the PWM unit 39 and power management unit 37.

Low load conditions at VOUT can be detected by the feedback signal FB, as described in US6385061. As described below, a first comparator in the control unit 41 receives the input FB and provides such detection by comparing FB with a fixed voltage level.

- In US6385061 cycles are skipped (i.e. there is a pause between bursts) by blocking the PWM if FB is below a certain voltage threshold, and if the FB is above this threshold the PWM is no longer blocked. By contrast, in the present invention, the control unit 41 includes in addition to the comparator for detecting low load conditions (i.e. a comparator which detects if FB is below a given level and in this case blocks the effect of the PWM 39, for example by switching off the bias which the PWM modulates and applies to the gate of the transistor 15), a second comparator which also receives FB and detects whether FB exceeds a second higher threshold level. If this is true, then the PWM is activated again.
- Therefore a hysteresis is implemented using the two comparators, one for switching off the bias and one for switching on the bias. The bias is provided to sinks and sources which can be implemented using current mirrors for powering the control unit 101 and can switch off the internal current supply of the sub-blocks.
- By switching off the bias the current consumption of the control system can be reduced. This is preferable since during the time that the PWM 39 is blocked there is no self-supply for the  $V_{cc}$ , and the monitoring unit 1 relies for power supply on the reserve in the capacitor  $C_{V_{cc}}$ . Therefore reducing the current consumption helps to reduce the required size of the capacitor  $C_{V_{cc}}$ .
- The frequency and duty cycle of the frames (bursts) during the burst mode depend on the load conditions and the spacing of the thresholds  $V_2$ ,  $V_3$ . This is in contrast to the burst mode described in US6385061, and in the embodiment of Fig. 1 the lowest reachable frequency for the frames is much lower.
- Once the burst mode is activated, current limiting is applied to ensure that the current through the transistor 15 never rises above a predetermined level (the second aspect of the invention). This is to avoid audible noise being generated in the transformer due to the high current within the frames (bursts) of the burst mode. A third comparator is provided which also receives FB as an input, and which upon the load rising turns off the current limiting.
- These features are better understood from Fig. 2 (a), which is a diagram of a second embodiment of the invention. Portions of the embodiment which are the

same as components of the first embodiment are given the same reference numerals and not otherwise described. In this case the control system 1 is replaced by a control unit 101 (except that the conventional start-up cell 35 is provided separately. The control unit 101 can be implemented as a single integrated circuit logic device.

The control unit 101, like the control system 1, draws its power from the  $V_{cc}$  input (the ground terminal of the control unit 101 is omitted from Fig. 2 (a) for simplicity). The control unit 101 receives only two control inputs: CS, which is indicative of the current through the transistor 15 and the primary winding 9 of the transformer 7, and FB obtained from the secondary side of the transformer 7 through the optocoupler 29. The input FB is fed to two comparators C2, C3, which each also receive a respective threshold voltage  $V_2$ ,  $V_3$ . The outputs of the comparators C2 and C3 are used to control the timing of the bursts in the burst mode as described below. A first flip-flop FF2 receives their outputs, and uses them to control the bias.

The output of the FF2 is further transmitted via a logic gate G1 to a flip-flop 3 which further receives the clock signal CLK. The output of the FF3 is the control signal Gate for the transistor 15. Thus, the transistor 15 is switched in dependence on the clock signal CLK (which provides the switching at a high regular frequency, and thus plays the role of the PWM of Fig. 1) and the input to FF1 from the logic gate 1 which in the burst mode inhibits the switching.

Fig. 2 (a) illustrates an embodiment in which the feedback signal is directly related to the power drawn by the load. Fig. 2 (b) shows an alternate implementation of the second embodiment of the invention of Fig. 2 (a) in which the feedback signal is inversely related to the power drawn by the load. If the power consumption at  $V_{out}$  is decreasing, VFB (the feedback voltage) is increasing, and visa versa. Therefore, the relationship between the threshold voltages  $V_{1a}$ ,  $V_{2a}$  and  $V_{3a}$  is the inverse of the thresholds  $V_1$ ,  $V_2$  and  $V_3$  of the implementation of Fig. 2 (a) where the feedback signal is directly related to the power drawn by the load. The relationship is  $V_{3a} > V_{2a} > V_{1a}$ . This same implementation method can be applied to circuits of Figs. 6 and 7 described

below. The signal curve for VFB is the inverse of those shown in Figs. 3, 5 and 8 below. In the implementation of Fig. 2 (b), RFB (the feedback resistance) is acting as a pull-down resistor that can also be replaced by an active current sink.

- 5 The performance of the device will now be described with reference to Fig. 3, which shows the variation of FB, CS and bias voltage as a function of time. Initially the load is high enough that the burst mode is not entered. At time  $T_1$  the load falls such that burst mode operation should be applied, but at a time  $T_2$  the load jumps back to a high level.
- 10 In the case of low load, whenever FB decreases below  $V_3$  (e.g. at time  $T_1$ ), the flip-flop FF2 immediately blocks the Gate signal via gate G1 and flip-flop FF3 and switches off the bias. As there is no longer PWM switching,  $V_{out}$  decreases and causes FB to rise. If FB exceeds  $V_2$ , FF2 is reset by the comparator C2 to switch on the bias and to release G1. The clock signal CLK can now start the
- 15 switching cycle by setting FF3. If the load is still low, FB decreases again below the threshold  $V_3$  and deactivates the bias again. Thus, there is a burst of spikes in the periods shown as  $T_{on}$  during which FB is decreasing between  $V_2$  and  $V_3$ , and then no spikes during the periods  $T_{off}$  in which FB is rising from  $V_3$  to  $V_2$ . The frequency of the bursts  $F_{burst}$  is the reciprocal of  $T_{on} + T_{off}$ .
- 20 The voltage FB is also transmitted to a comparator C1, which further receives a threshold voltage  $V_1$  which is higher than both  $V_2$  and  $V_3$ . The passage of FB above  $V_1$  indicates that the burst mode is ended. A flip flop FF1 stores the value output from the comparator C1 until this is reset by the comparator C1. Thus, the output of FF1 is a signal indicating whether the burst mode is
- 25 currently being operated.

Note that in this embodiment this signal is not transmitted directly to the gate G1. Instead, the output of FF1 is used as an input to a system at the lower right of the control unit 101 including a first comparator C4 which compares the input CS to a threshold voltage level  $V_4$ , and transmits the output to the logic gate

30 G2.

Thus, at the same time that the C2 controls the flip-flop FF2 to block the PWM, it allows the FF1 to release the output of C1, which in turn allows the gate G2 to release the output of the comparator C4.

In other words, logic gate G2 outputs an input to the logic gate G1 in the case that the comparator C4 finds that the CS indicates that the current through the transistor is above a predetermined level (a level such that CS is at least  $V_4$ ) and the FF1 indicates that the power converter is operating in the burst mode. In the case that both of these are true, the output of the gate G1 has the effect of turning off the current through the transistor 15. This is illustrated in Fig. 4, which shows the profile of a single triangular current spike in the burst mode (line 37), in comparison to a single triangular current spike (line 39) when the burst mode is not being operated. When the current rises above  $V_4$  in the burst mode, it is promptly shut-off by turning the transistor 15 off.

If there is a load jump, as at time  $T_2$ , FB will immediately exceed  $V_2$  and then rise further, since due to the current limiting performed by the comparator C4, the current provided is not sufficient for the sudden power demand. If FB exceeds  $V_1$ , FF1 is reset, and the output of the comparator C4 is blocked by G2. In this case the maximum current is limited by the comparator C5 which compares CS with a second threshold  $V_5$  (higher than  $V_4$ ), and shuts off the current when CS is above  $V_5$ . A high power is therefore delivered to the load very promptly. A comparator with the function of C5 is known from US6385061.

The device then enters a normal operating mode (as in conventional systems) in which FB does not fall below  $V_3$ , so the burst mode is not re-entered (until the load drops again).

Note that, due to the hysteresis provided by the comparators C2 and C3, when the device is operating in the burst mode the bursts have the highly desirable property shown in Figs. 5(a)-5(b). The upper part of Fig. 5(a) shows the profile of FB in a low load state, while the lower part of Fig. 5(a) shows the corresponding pattern of spikes. The upper part of Fig. 5(b) shows the profile of FB in a high load state, while the lower part of Fig. 5(b) shows the corresponding pattern of spikes. Although the duty cycles of the spikes in the

lower parts of Fig. 5(a) and Fig. 5(b) are different, they have the same fundamental frequency,  $f_{\text{Burst}}$ . Fig. 5(c) shows a plot  $f_{\text{Burst}}$  against load, and demonstrates that  $f_{\text{Burst}}$  rises to a maximum and then falls. This is in contrast to the system shown in US6385061 (which employs only a single comparator),  
 5 since there as the load rises  $f_{\text{Burst}}$  rises too, to the point at which it enters the audible range, at which point an unpleasant audible noise may be generated.

Figure 6 shows a modified implementation of the embodiment of Fig. 2 (a), differing only in that the threshold terminals of comparators C3 and C4 are connected to pins of the logic device which implements the control unit 101.  
 10 This means that the thresholds V3 and V4 can be adjusted by external connected voltage references, or external connected resistors, thus determining the thresholds of C3 and C4.

Another possible variation of the embodiment of Fig. 2 (a) (or of Fig. 6) would be to connect a current source to FB in the place of the pull-up resistor  $R_{\text{FB}}$ .

15 Fig. 7 shows a further embodiment of the invention, and Fig. 8 shows the associated signal curves. The embodiment of Fig. 7 permits an adjustable blanking time window. If the power converter is initially not in the burst mode and a sudden high load causes FB to fall below V3, the burst mode will not be entered provided that FB is below V3 for a time less than this blanking window.

20 The blanking time window is realised by the additional gates G3, G4, G5, G6 and a comparator C6, a switch S1, a Zener diode  $V_z$  and an external capacitor C1. The gate G5 opens the switch S1 when a NAND of the output of FF2 and the inverse of C3 is one. The other gates have the functions shown in Fig. 7.

25 The capacitor C1 is charged by the internal pull-up resistor R2, which is connected to a reference voltage  $V_{\text{ref}}$ . If FB decreases below V3 while the output of FF2 is low, the output of C3 becomes high, so the switch S1 is opened by G5.

30 If FB remains below V3, then  $V_{\text{Softs}}$  increases until  $V_6$ . In this case G3 is released, and FF2 is set if FB is still below V3.

Conversely, if FB exceeds  $V_3$  in the when FF1 is not set, then S1 will be closed and  $V_{SoftS}$  is clamped again at  $V_z$ , and the burst mode is not entered. Note that nevertheless the data in FF1 means that current limitation is applied.

5

If FF2 is set, then the burst mode is entered, and S1 is closed by FF2 and cannot be opened by C3. This ensures that the blanking time window function only works before the burst mode is entered.

10 G3, G4 and G6 collectively provide the function that the input to FF1 is only 1 if the outputs of the comparators C3 and C6 are both positive (indicating that the blanking time window has been passed) and/or the output of comparator C3 and of the FF2 itself are both positive (indicating that the FB is less than  $V_3$  and that the device is already inhibiting PWM, and thus is already in the burst  
15 mode).

Note that many variations of this embodiment are possible too. For example, in this embodiment, the pull-up resistor R2 can be replaced by an internal current source.

20

It is also possible to fully integrate the components which implement the blanking time window into the control unit 101, so that no pin is required, for connection to an external capacitor (i.e. C1 is located within the logic device which implements control unit 101). The time constant is internally fixed in this  
25 case. This can be realised by an internal capacitor which is charged by an internal current source. If a large time constant is required, a digital counter can provide it, the digital counter replacing the internal capacitor.

Thus, although the invention has been described above using particular  
30 embodiments, many variations are possible within the scope of the claims, as will be clear to a skilled reader.

Claims

1. A switching mode power supply having a transformer, a transistor controlling the current through a primary of the transformer, and a control unit for controlling the switching of the transistor to generate current pulses in the transformer, the control unit being arranged to receive a signal from the secondary side of the transformer and compare it with two threshold levels defining a range, the control unit enabling switching of the transistor in the case that the signal is outside the range in a first direction, and disabling switching of the transistor in the case that the signal is outside the range in a second direction.
2. A switching mode power supply according to claim 1 in which the signal is inversely related to the power drawn by the load, and the control unit enables switching when the signal is above a first threshold value, and disables switching of the transistor in the case that the signal is below a second lower threshold value.
3. A switching mode power supply according to claim 1 in which the signal is directly related to the power drawn by the load, and the control unit enables switching when the signal is above a first threshold value, and disables switching of the transistor in the case that the signal is below a second lower threshold value.
4. A switching mode power supply according to claim 1, claim 2 or claim 3 further comprising a blanking window definition circuit which prevents the control unit for disabling switching of the transistor in the case that the signal is below the second lower threshold value for less than a preset period of time.
5. A switching mode power supply according to claim 1, claim 2, claim 3 or claim 4 further comprising a current limitation circuit arranged to receive an signal indicative of the current through the primary of the transformer and to limit the current pulse if the signal indicates that the current is above a threshold value.

6. A switching mode power supply according to claim 5 having a memory device for storing data indicating whether the switching mode power supply is operating in a certain power supply mode, and arranged to enable the current limitation circuit only in the case that the power supply is operating in that power supply mode.
7. A switching mode power supply having a transformer, a transistor controlling the current through the primary of the transformer, a control unit for controlling the switching of the transistor to generate current pulses in the transformer, a memory device for storing data indicating whether the switching mode power supply is operating in a certain power supply mode, and a current limitation circuit arranged to receive an signal indicative of the current through the primary of the transformer and to limit the current pulse if the signal indicates that the current is above a threshold value and the memory device indicates that the switching mode power supply is operating in said power supply mode.
8. A switching mode power supply according to any preceding claim in which the control unit is a single integrated circuit logic device.
9. A switching mode power supply according to claim 8 in which at least one of the threshold values is determined by a pin input of the logic device.
10. A switching mode power supply according to claim 8 or claim 9 in which at least one of the threshold values is determined by an internal reference voltage of the integrated circuit.
11. An apparatus incorporating and powered by a switching mode power supply according to any preceding claim.
12. A method of operating a power supply having a transformer, a transistor controlling the current through the primary of the transformer, and a control

unit for controlling the switching of the transistor to generate current pulses in the transformer, the method including:

receiving a signal from the secondary side of the transformer and comparing it with two threshold levels, and

5 enabling switching of the transistor in the case that the signal is outside the range in a first direction, and disabling switching of the transistor in the case that the signal is outside the range in a second direction.

13. A method of operating a power supply having a transformer, a transistor controlling the current through the primary of the transformer, and a control  
10 unit for controlling the switching of the transistor to generate current pulses in the transformer, the method including:

receiving an signal indicative of the current through the primary of the transformer and,

15 in the case that the power supply is operating in a certain power supply mode, to limit the current pulse if the signal indicates that the current is above a threshold value.

**ABSTRACT**

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\*G00002\*

Switching mode power supplies

- 5 In a switching mode power supply, an input received from the secondary side of the transformer 7 and indicative of the power being drawn by the load is used to control the timing of bursts. The input is compared with two threshold different threshold values V2, V3, and switching is enabled if the input rises above a first higher threshold value V2, and disabled if it falls below a second lower
- 10 threshold value V3. A memory device FF1 controls a current limitation circuit which limits currents in the primary of the transformer when the switching mode power supply is operating in the burst mode.

Fig. 1



**\*163163\***



**\*G00002\***

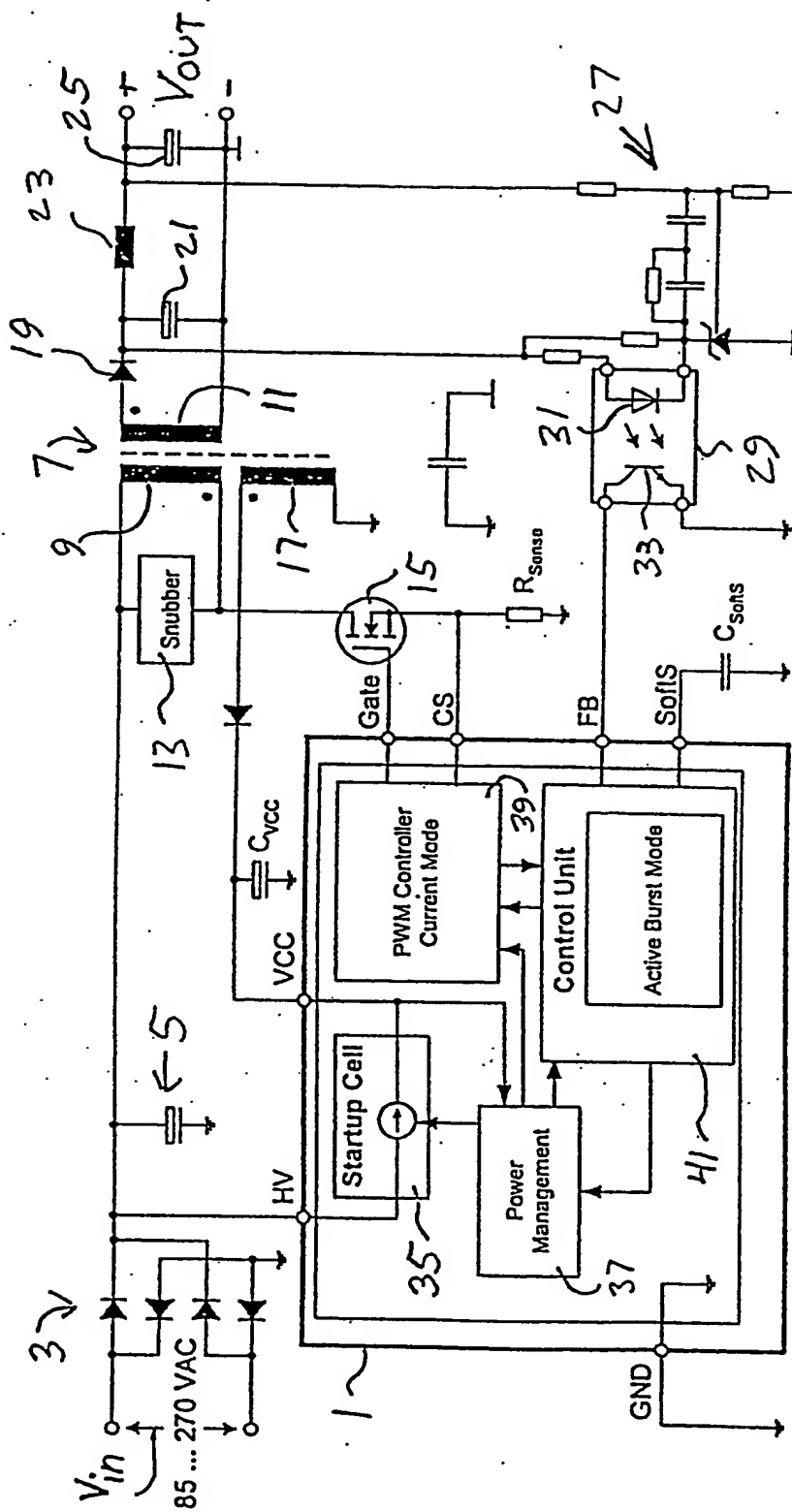


FIG. 1

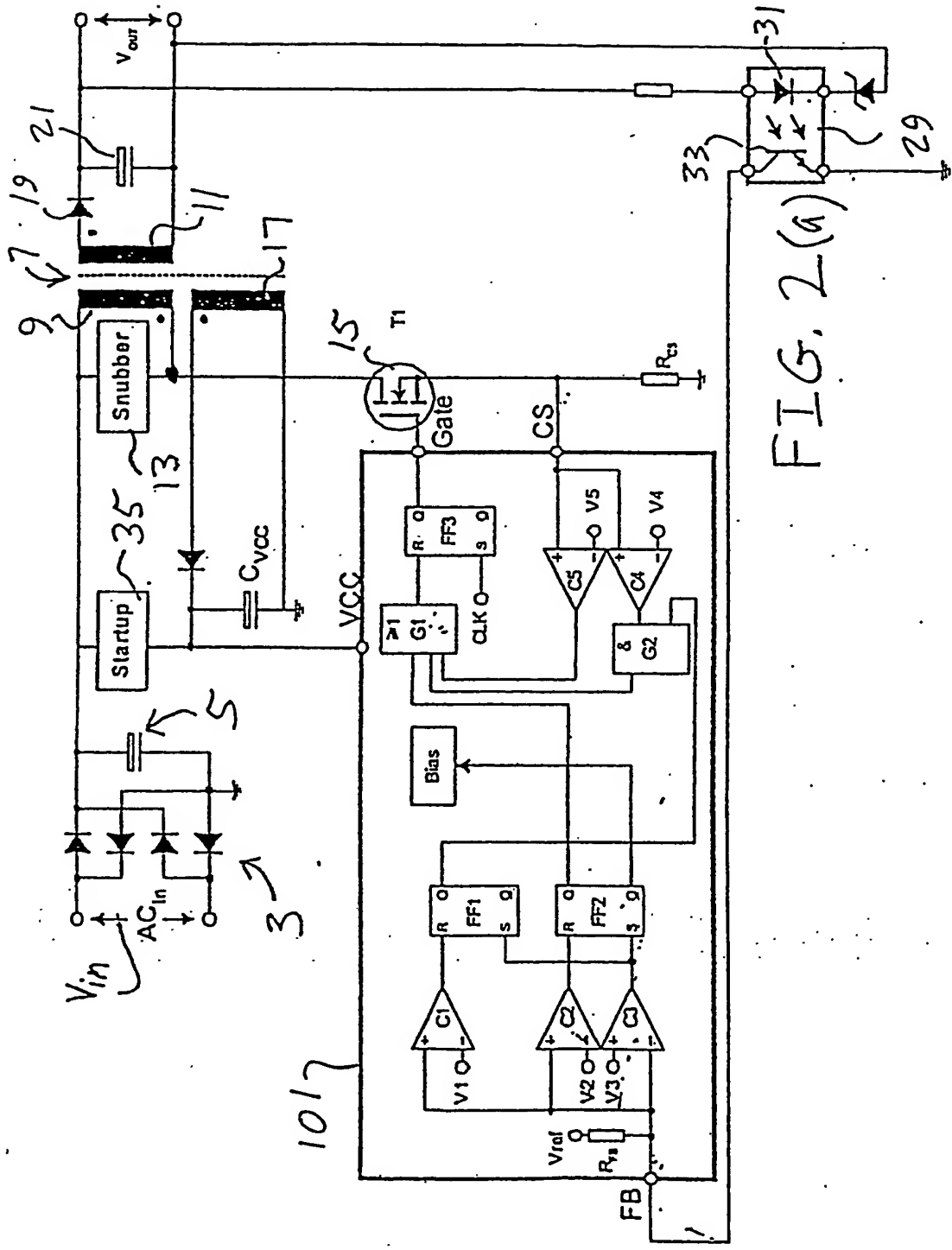


FIG. 2(a)



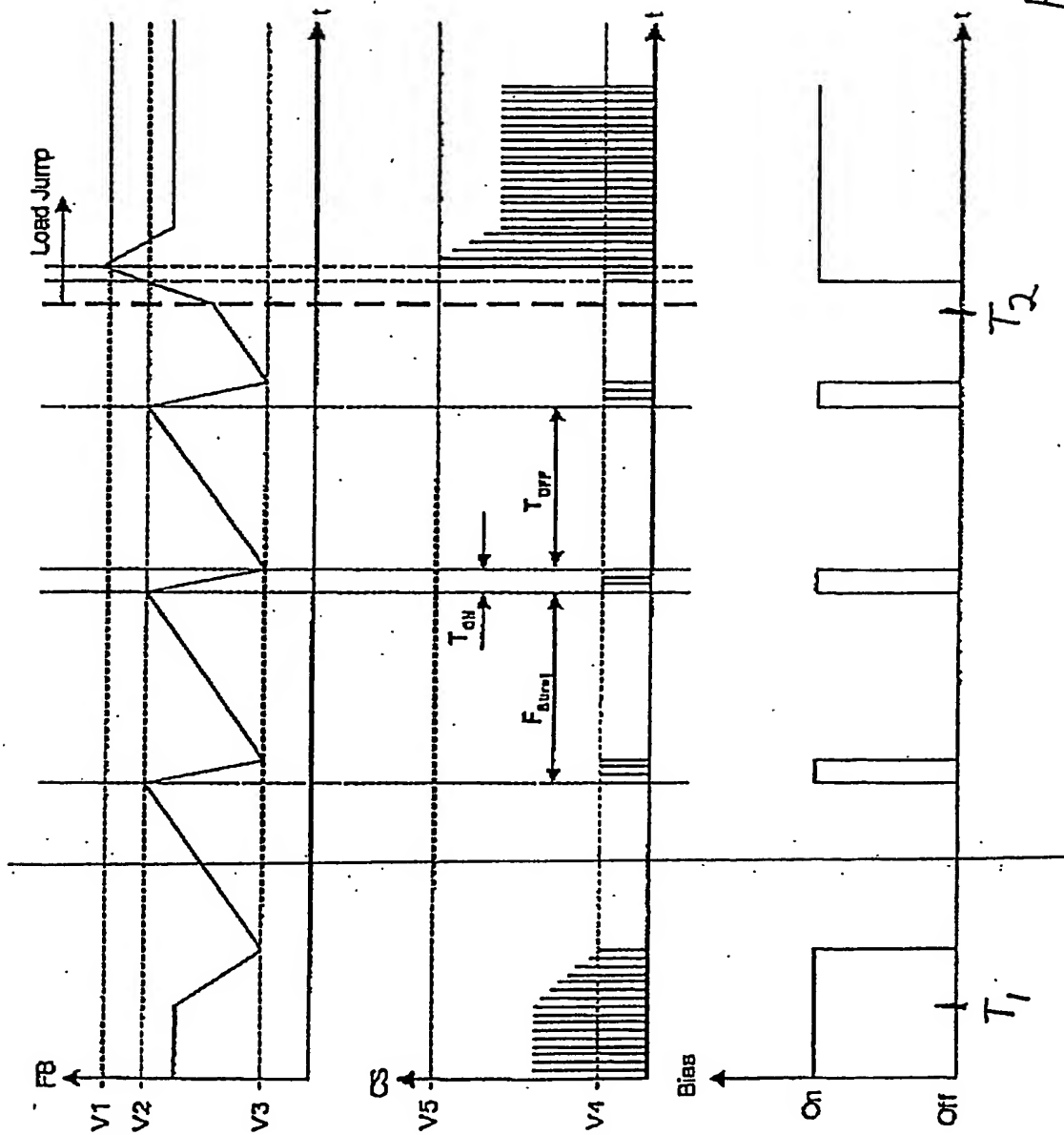


FIG. 3

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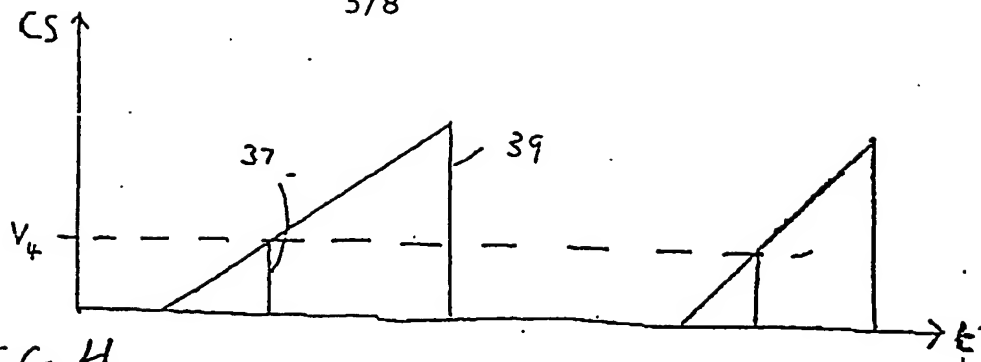


FIG. 4

Fig. 5(a)

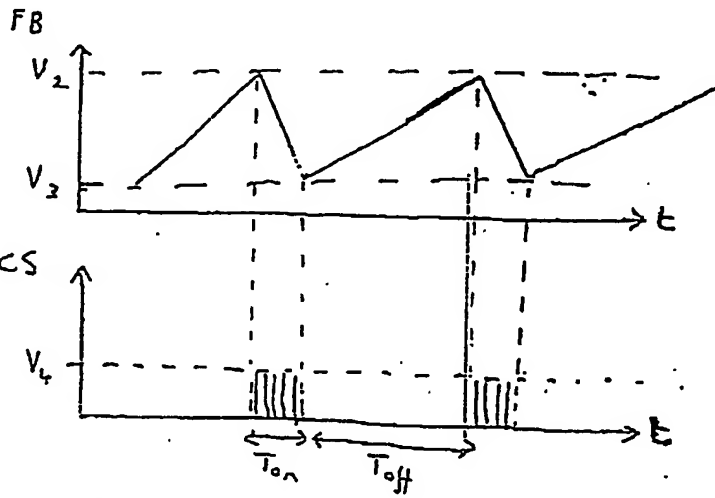


Fig. 5(b)

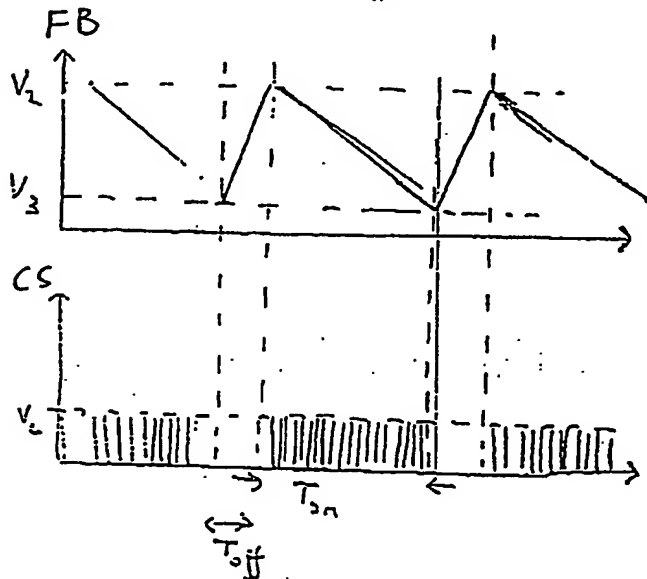
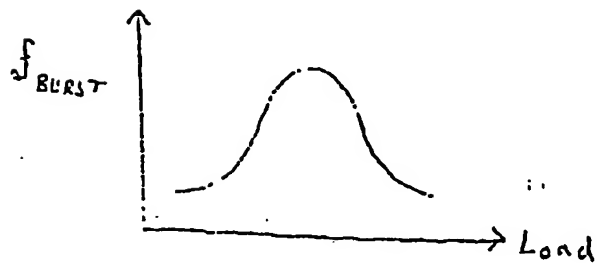
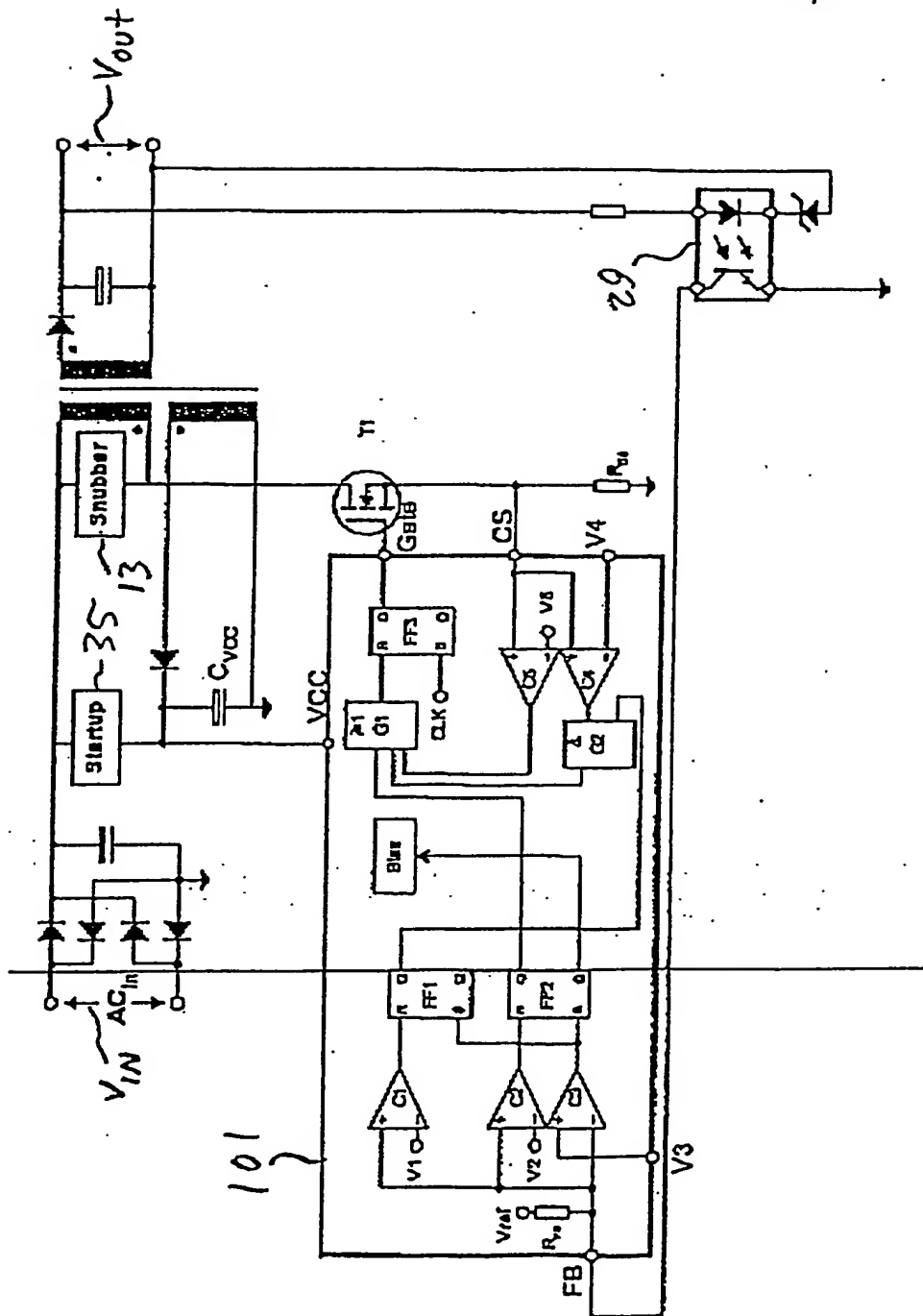


Fig. 5(c)





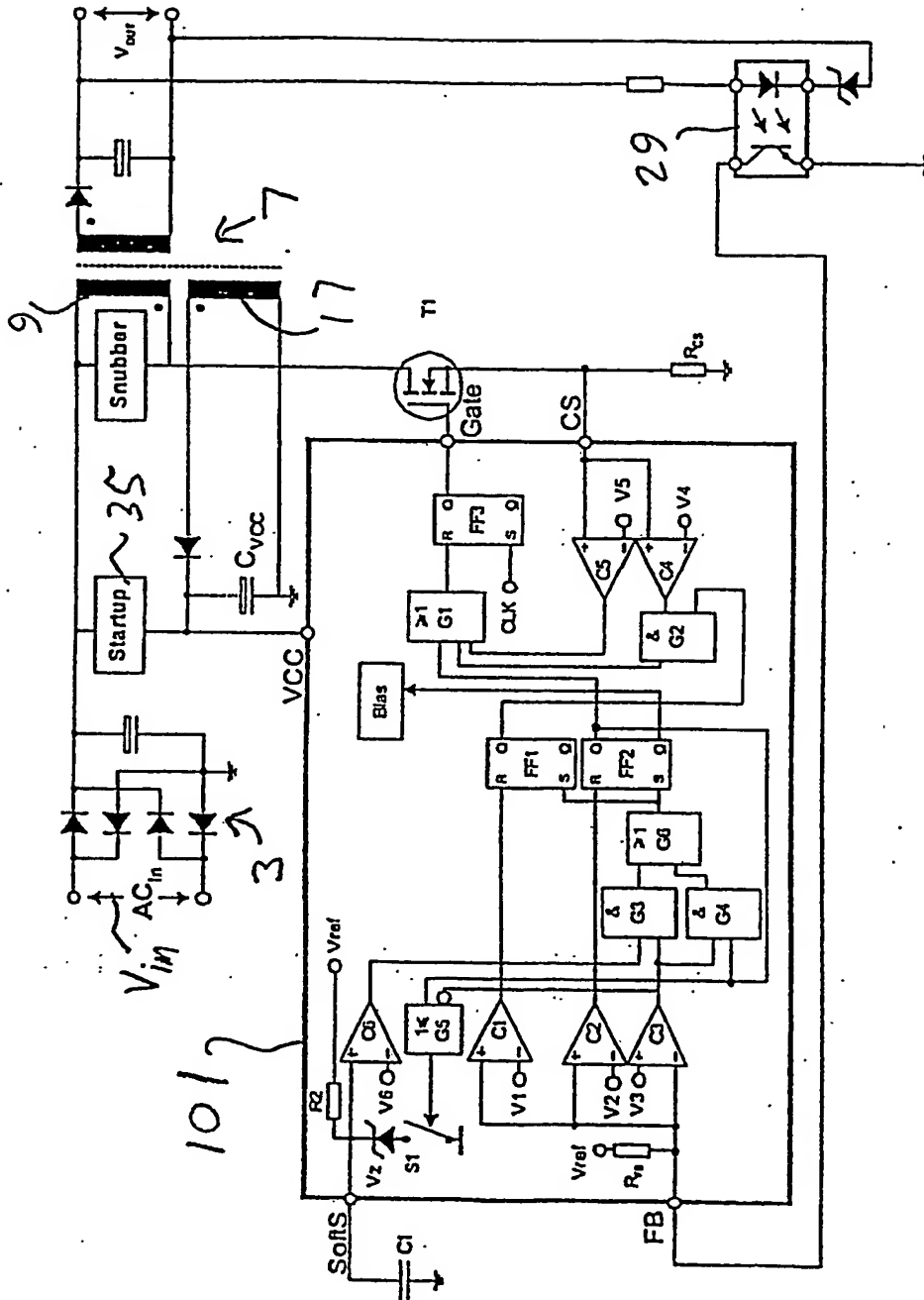


FIG. 7

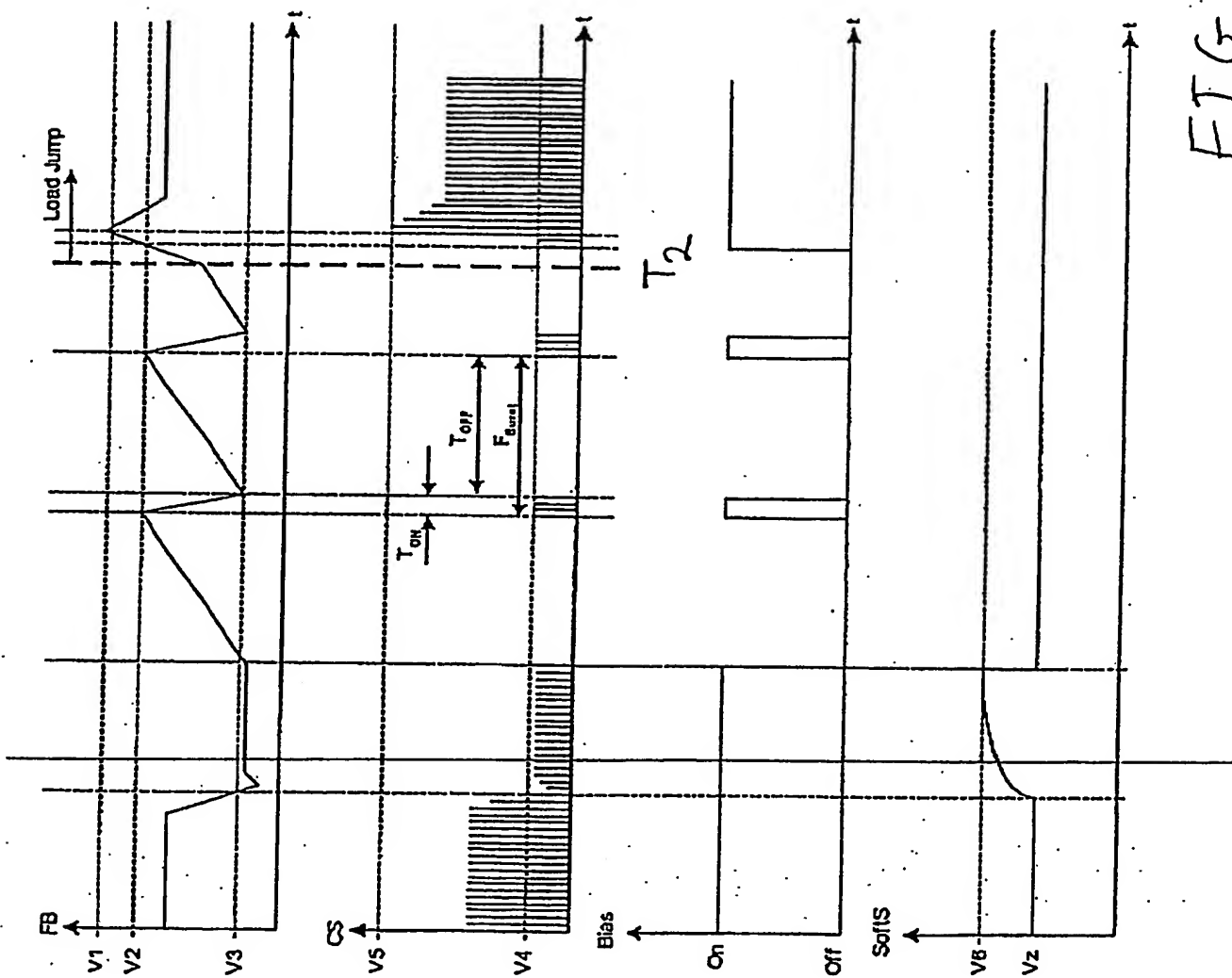


FIG. 8

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